

CLAIMS

- 1 1. A method of bonding lattice-mismatched semiconductors comprising;
2 forming a Ge-based virtual substrate;
3 depositing on said virtual substrate a CMP layer that is polished to form a
4 planarized virtual substrate;
5 bonding a Si substrate to said planarized virtual substrate;
6 performing layer exfoliation on selective layers of said planarized virtual substrate
7 producing a damaged layer of Ge; and
8 removing said damaged layer of Ge.
- 1 2. The method of claim 1, wherein said virtual substrate comprises an etch-stop layer.
- 1 3. The method of claim 1, wherein said virtual substrate comprises a III-V transfer layer.
- 1 4. The method of claim 3, wherein said III-V transfer layer serves as an etch-stop.
- 1 5. The method of claim 1, wherein said virtual substrate comprises a $\text{Si}_{1-x}\text{Ge}_x$ passivation
2 layer.
- 1 6. The method of claim 1, wherein said virtual substrate comprises a Si_3N_4 passivation
2 layer.
- 1 7. The method of claim 1, wherein said CMP layer comprises an oxide.
- 1 8. The method of claim 1, wherein said CMP layer comprises Si.
- 1 9. The method of claim 2 further comprising removing said etch-stop layer after
2 removing said damaged Ge layer.

- 1 10. The method of claim 9, wherein said etch-stop comprises $\text{Si}_{0.4}\text{Ge}_{0.6}$.
- 1 11. The method of claim 9, wherein said virtual substrate comprises at least one relaxed
2 Ge layer and SiGe buffer.
- 1 12. A method of bonding lattice-mismatched semiconductors comprising;
2 forming a virtual substrate;
3 using said virtual substrate to form a planarized virtual substrate;
4 bonding a Si substrate to said planarized virtual substrate; and
5 removing selective layers of said planarized virtual substrate associated with said virtual
6 substrate.
- 1 13. The method of claim 12, wherein said virtual substrate comprises an etch-stop layer.
- 1 14. The method of claim 12, wherein said virtual substrate comprises a III-V transfer
2 layer.
- 1 15. The method of claim 14, wherein said III-V transfer layer serves as an etch-stop.
- 1 16. The method of claim 12, wherein said virtual substrate comprises a $\text{Si}_{1-x}\text{Ge}_x$
2 passivation layer.
- 1 17. The method of claim 12, wherein said virtual substrate comprises a Si_3N_4 passivation
2 layer.
- 1 18. The method of claim 12, wherein said planarized virtual substrate is formed using
2 oxide.

- 1 19. The method of claim 12, wherein said wherein said planarized virtual substrate is
2 formed using $\text{Si}_{1-x}\text{Ge}_x$.
- 1 20. The method of claim 13 further comprising removing said etch-stop layer after
2 removing said damaged Ge layer.
- 1 21. The method of claim 20, wherein said etch-stop comprises $\text{Si}_{0.4}\text{Ge}_{0.6}$.